# DFM Rules for BGA's

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August 2012

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The Product Realization Company

# DFM Guidelines for BGA's and LGA's

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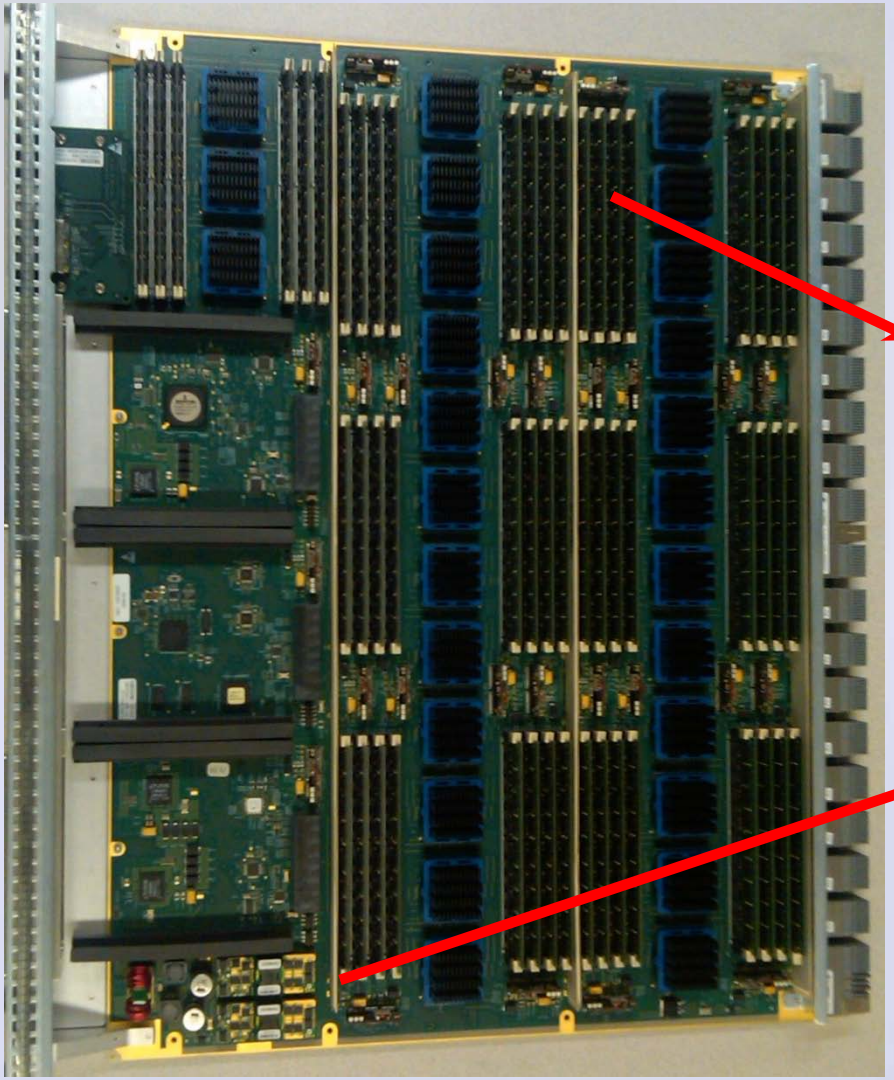
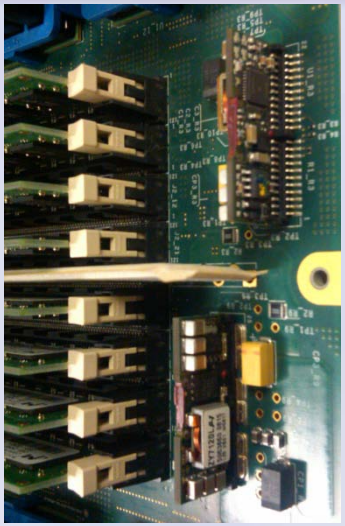
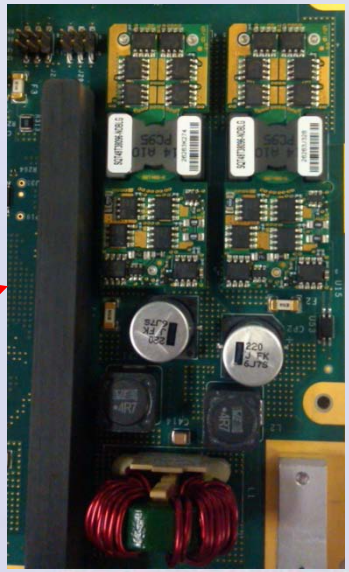
# Today's Electronics

- High Layer Counts
- Wide Range Of Component Package Sizes
- Soldered Other Soldered Assemblies
- Mixed SMT & PTH Technology
- Increased Component / Interconnection Density
- Higher Number Of Components (10,000 Plus)







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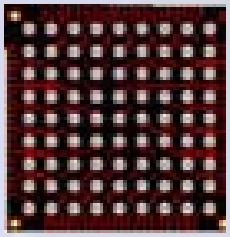
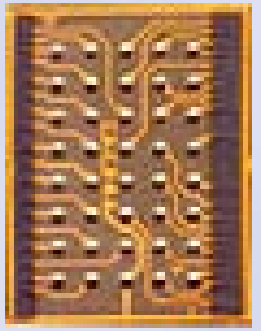
# Area Array Packages



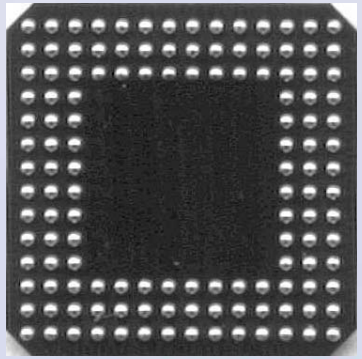
0.8mm Flex CSP

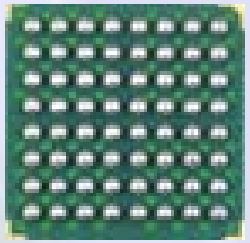
0.5mm u-SMD



0.75mm Flex CSP

1.0mm Flex CSP





1.0mm Laminate CSP

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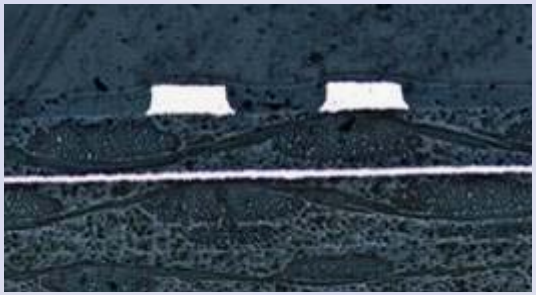
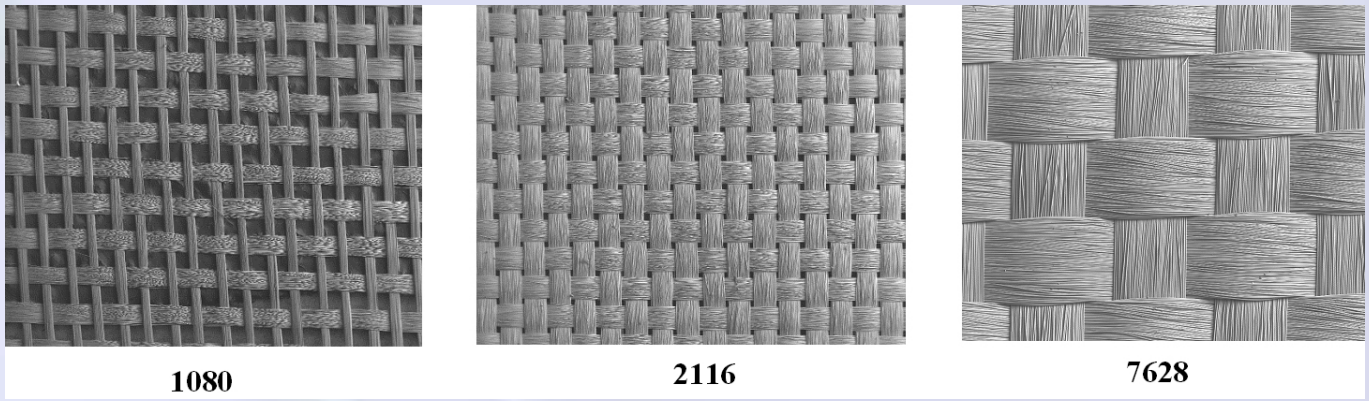
# PCB Laminate Construction

- Laminate Made From Mix of Resin & Glass
- Most Common Types: 7628HR, 7628,2116, 2113,1080,1080LD,106
- Location of Trace to Glass (Dk~6) Bundle or Resin (Dk~3.5) Pocket Can Impact Electrical (Impedance) And Mechanical Performance



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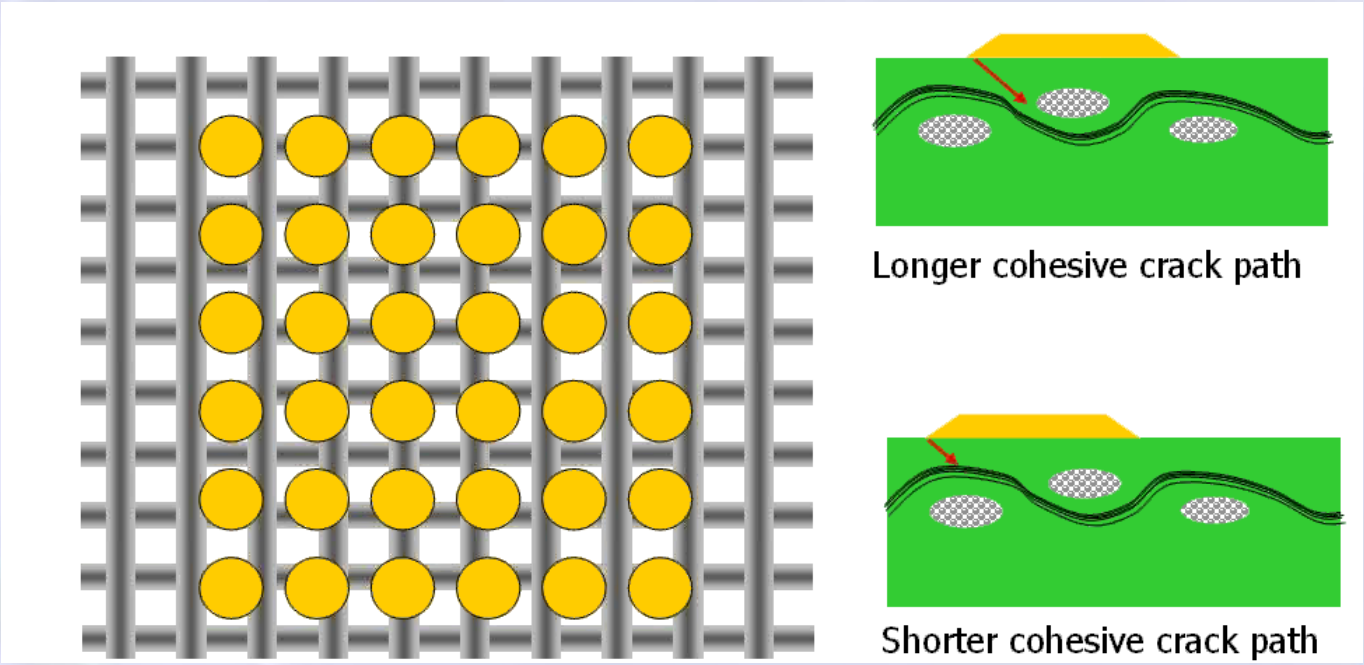
# Pad To Glass Bundle Interaction

- Location of Pad Relative to Glass Has An Impact On:
  - Crack Location & Formation
  - Functional Performance
- Size And Shape Of Pad Also Important Factor




Courtesy of Universal Instruments

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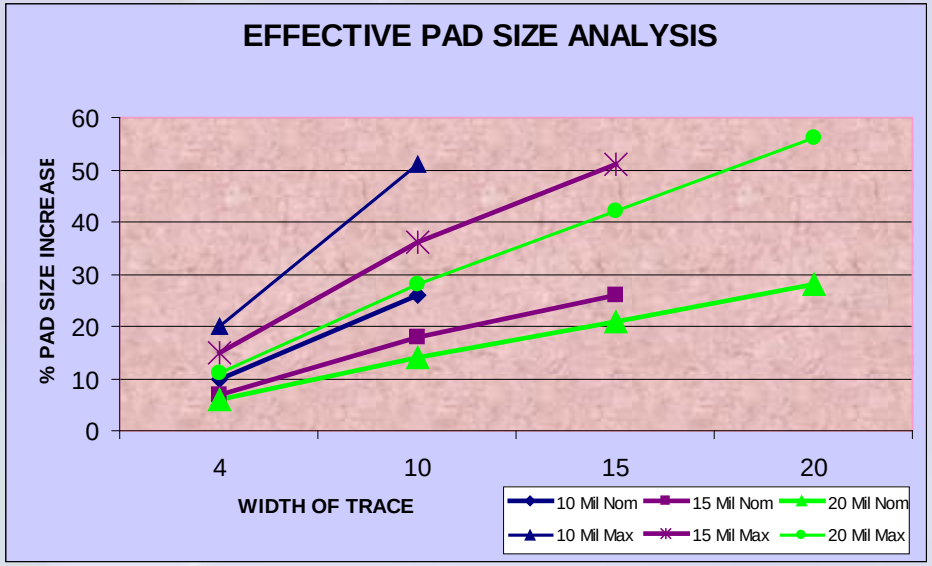
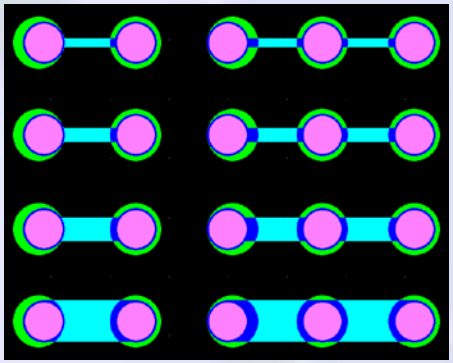
# SMT Component Land Pattern

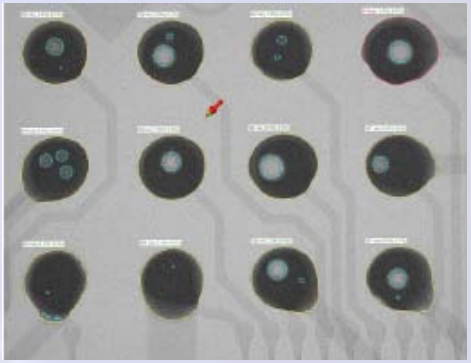
When developing a new land pattern design, utilize pad design recommendations from suppliers with volume production experience first. If no recommendation is available refer to IPC-7351 (Surface Mount Design and Land Pattern Standard) as a comprehensive land pattern design guide starting point.

All new land pattern designs should be tested in an actual production environment prior to release as a production design standard.

# Trace Routing Impacts Solder Joint





## Increased Mounting Pad Size Affected By:

- Number Of Trace Connections To Each Pad
- Width Of Trace Connections To Each Pad
- Size of Pad
  - Small Pads Have Less Margin
- Uniformity Of Trace Egress Direction
  - Some Package Types Are More Sensitive Than Others
- Uniformity Of Trace Sizes

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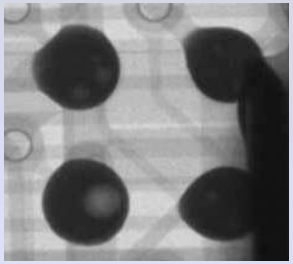
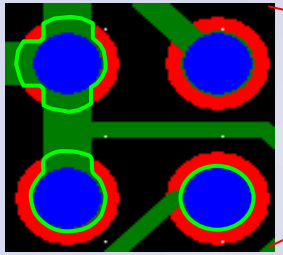
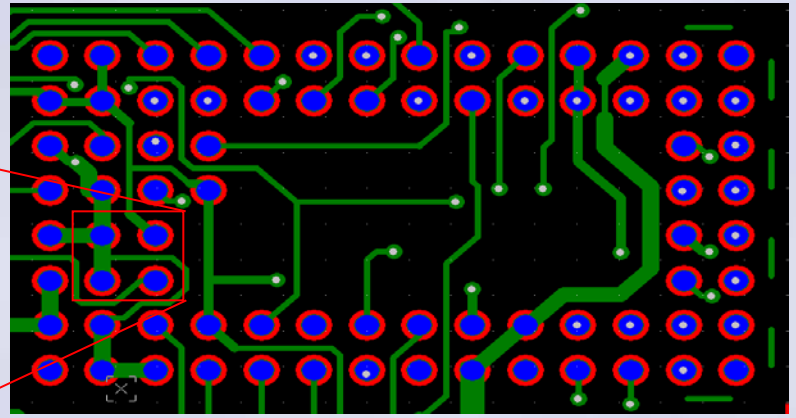
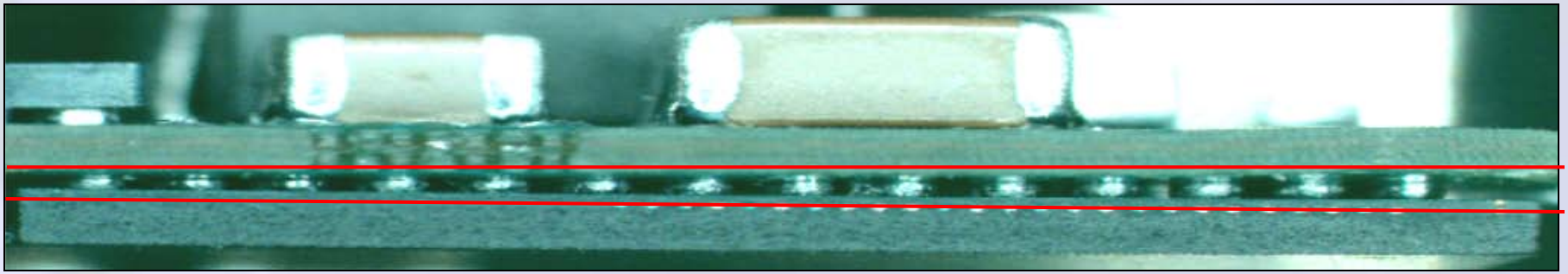
# Trace Routing Impacts Solder Joint

- Gradient Of Different Trace Sizes
- Localized Concentrated Large Trace Connections Increase Defect Potential









- Concentrations Of Design Variability Can Create:
  Solder Bridge, Open Connection, Insufficient Solder, Tilted Components

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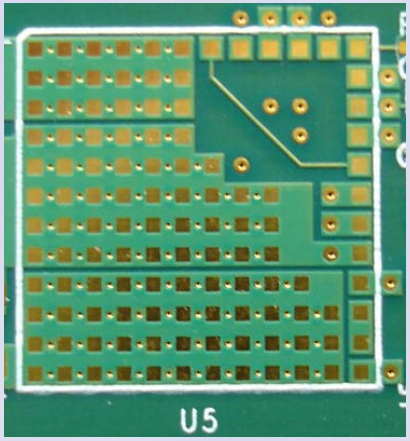
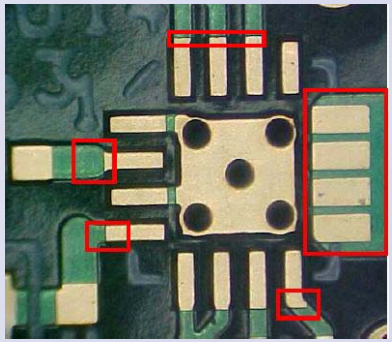
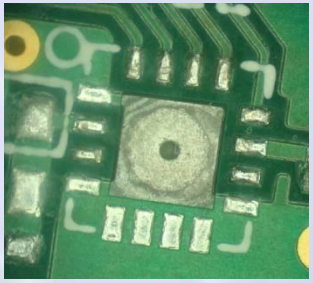
# Component Issues – LGA & QFN

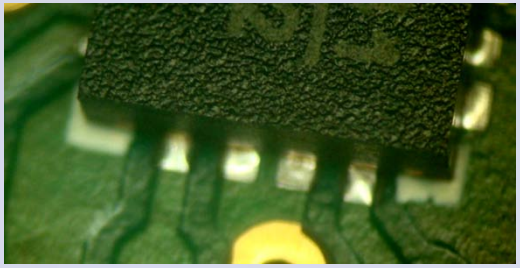
**Potential Issues:**

- Land Pattern Design
  - Pad Size Uniformity (SMD vs NSMD)
- Paste Volume Control
  - Pad to Pad Volume
  - Pad to Design Defined Volume
- Component/PCB Flatness
  - Internal Split Plane
  - NFP Removal Impacts
- Component/PCB Warpage
- Decrease Component Standoff Height
  - Decreased Reliability







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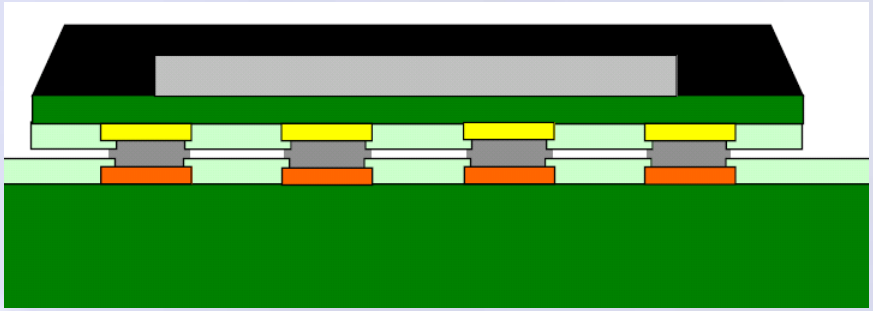
# LGA Pad Design

Solder Mask Defined

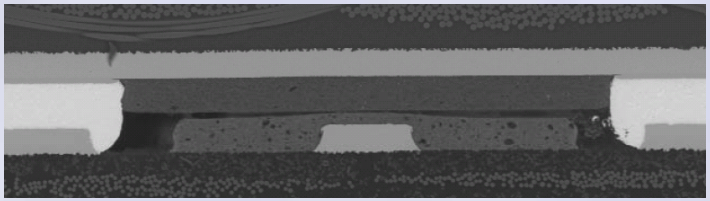
Non-Solder Mask Defined

- Solder wicking around NSMD pads produce significantly lower molten solder height.
- Solder mask defined pads should be used for LGA and 0.4mm & smaller pitch BGA/CSP packages.



# LGA/QFN Package Assembly

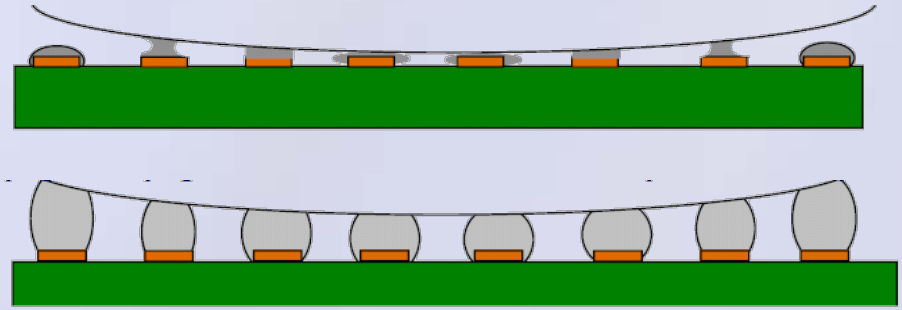
- Trace Routing Under Component Create Localized Height Variations
  - Standoff Height Variation



- Leadless Devices Are More Sensitive To PCB/Component Flatness/Warpage
  - Received Condition
  - In-process Condition (During Reflow/Rework Solder Process)

LGA Package

BGA Package



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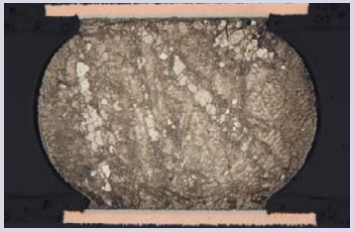
# Component Issues – Decreasing Pitch

- 0.2 mm

- 0.4 mm



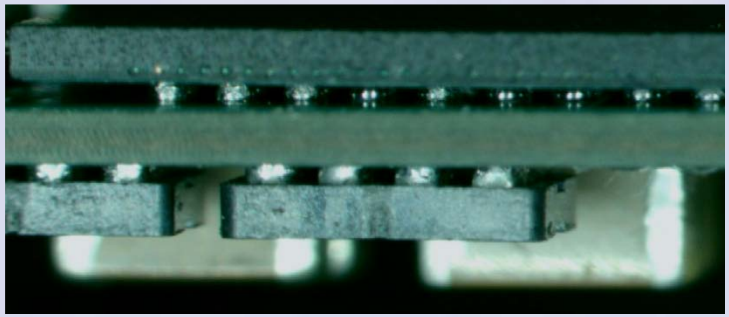
- 0.8 mm

- 1.0 mm

- 1.27 mm

## Potential Issues:

- Paste Volume Control
- Component/PCB Flatness
  - Internal Split Plane
  - NFP Removal Impacts
- Component/PCB Warpage



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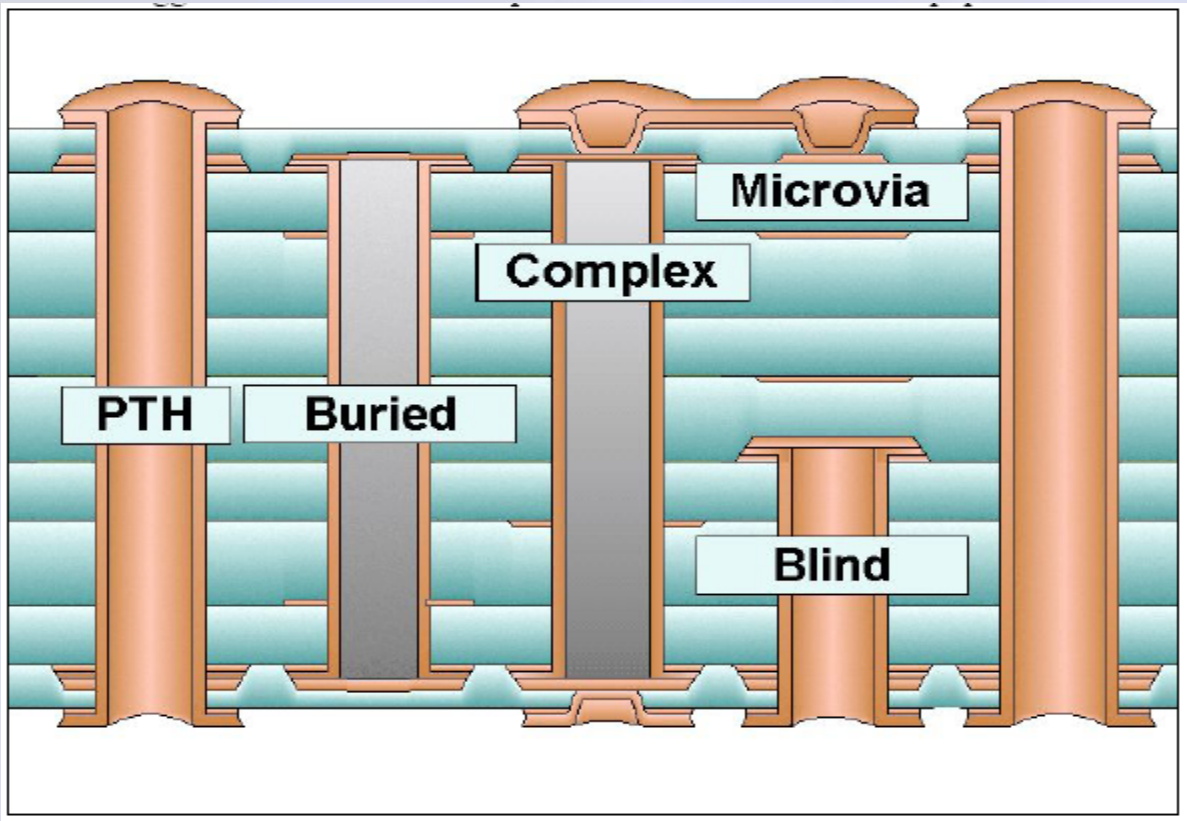
# Impacts of Via Design on Assembly

- Placement And
  - Types Of Vias In Pad Can Affect Assembly Solder Joint Formation
    - More Of An Impact On Smaller Components And/Or Lower I/O Count




Design and Construction Affects on PWB Reliability, Paul Reid, IPC Apex Proceedings 2012.

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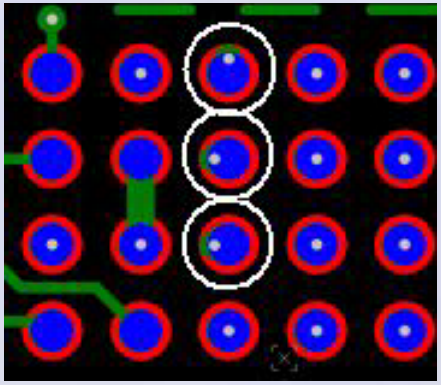
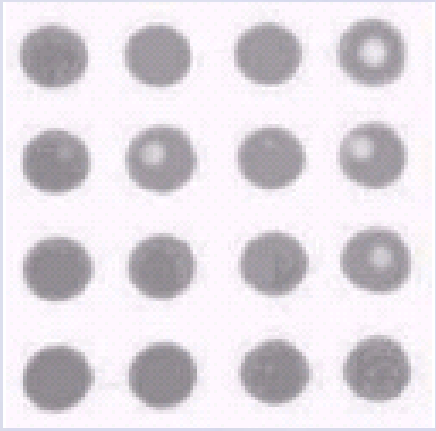
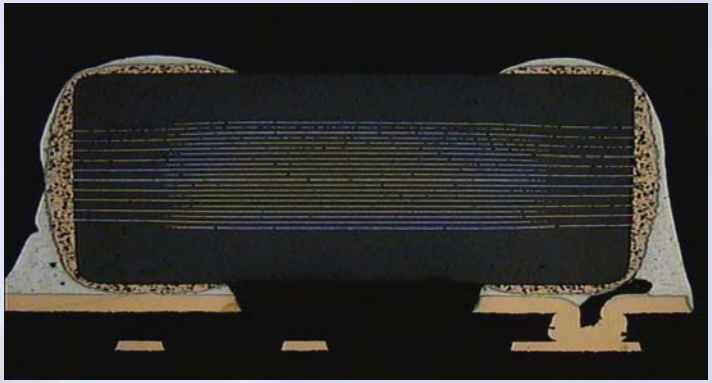
# Micro-Via in Pad

- Micro-Via Locations Should Be Consistent
  - Area Array Components - Center of Pad
  - Leadless (Chips, Chip Array, LCC, QFN, etc) and Leaded (QFP, SOIC, SOT, etc.) Components – Near Toe Fillet





X-ray Image



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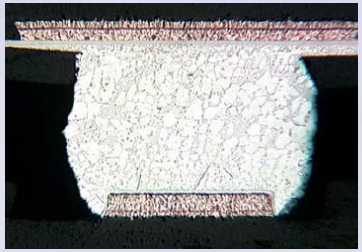
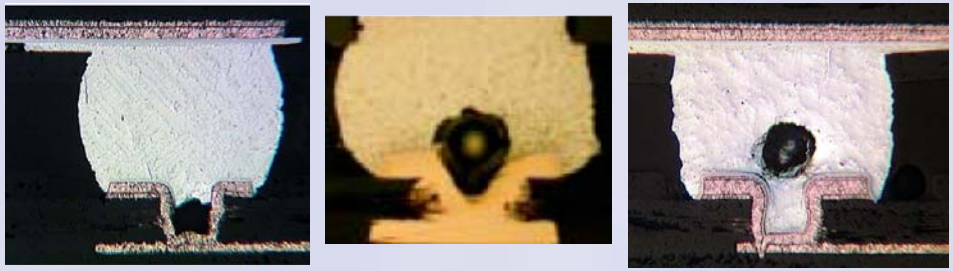
# Micro-Via in Pad

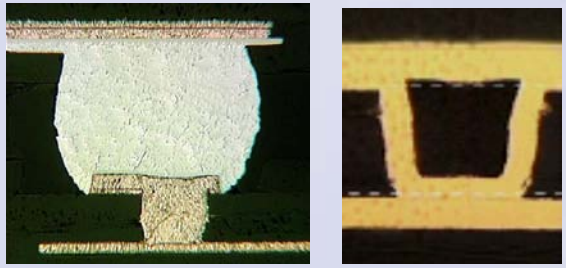
- Voids in Solder Joints
  - Unfilled Via in Pad
- Provide Flat Pad With Filled/Plated Closed Via
- Solder Joint Formation
  - Thermal Connection
    - Plane Connection
    - Multiple Connections
    - Stacked Via
  - Solder Volume
    - Via Location - Edge



No Via



Unfilled Via's



Plated Closed & Filled Via

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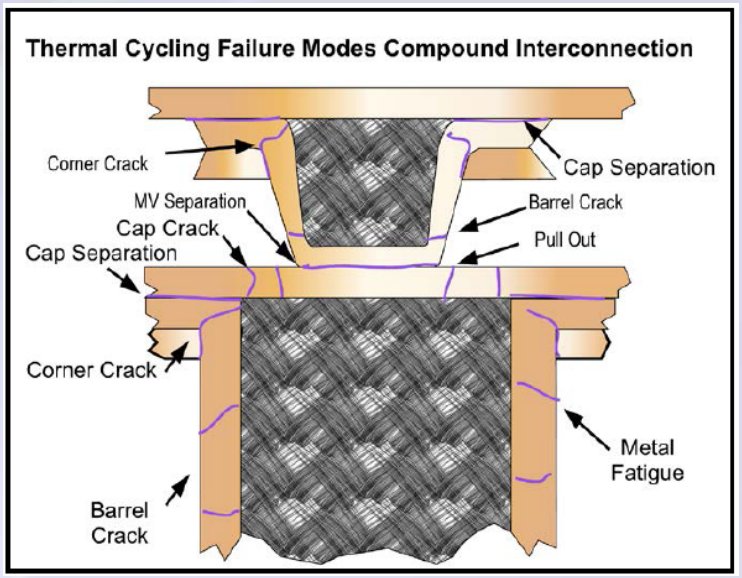
# Micro-Via Design – Reliability Impacts




| IST Cycles to Failure - Tested at 190°C | | | | | | |
|---|---|---|---|---|---|---|
| Precon | As Received | | | Predoncitioning 6X260°C | | |
| Type | Buried | Microvia | | Buried | Microvia | |
| Circuit | Power | Staggered | Stacked | Power | Staggered | Stacked |
| Mean | 1000 | 1000 | 79 | 1000 | 887 | 3 |
| StDev | 0 | 0 | 32 | 0 | 182 | 0 |
| Min | 1000 | 1000 | 52 | 1000 | 582 | 3 |
| Max | 1000 | 1000 | 138 | 1000 | 1000 | 3 |
| Range | 0 | 0 | 86 | 0 | 418 | 0 |
| Coef Var | 0% | 0% | 41% | 0.0 | 0.2 | 0.0 |

Different Via Hole Structures Impact Resistance To Assembly, Rework or Handling Damage

Design and Construction Affects on PWB Reliability, Paul Reid, IPC Apex Proceedings 2012.

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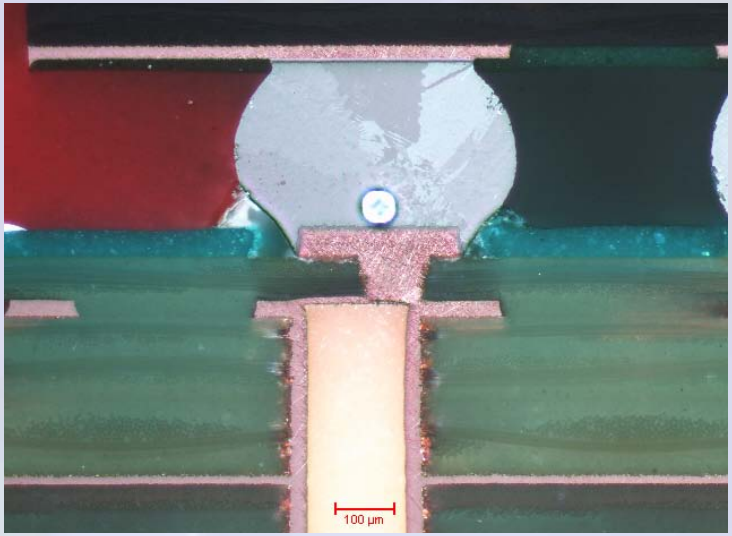
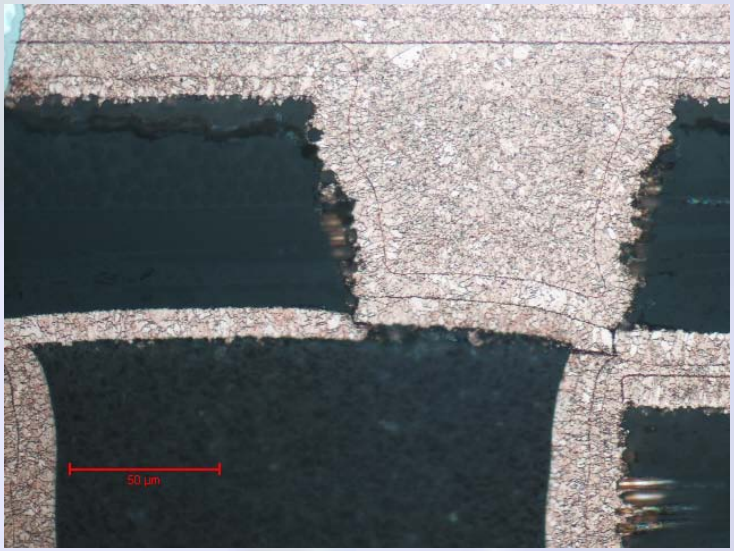
# Stacked Via In Pad Failure Mode




- Lead Free Laminate Is Less Ductile
- Lead Free Solder Is Less Ductile
- Increased Stress Transmission To Internal Connections
  - Test Fixture
  - Assembly Fixtures
  - System Integration
  - Environmental

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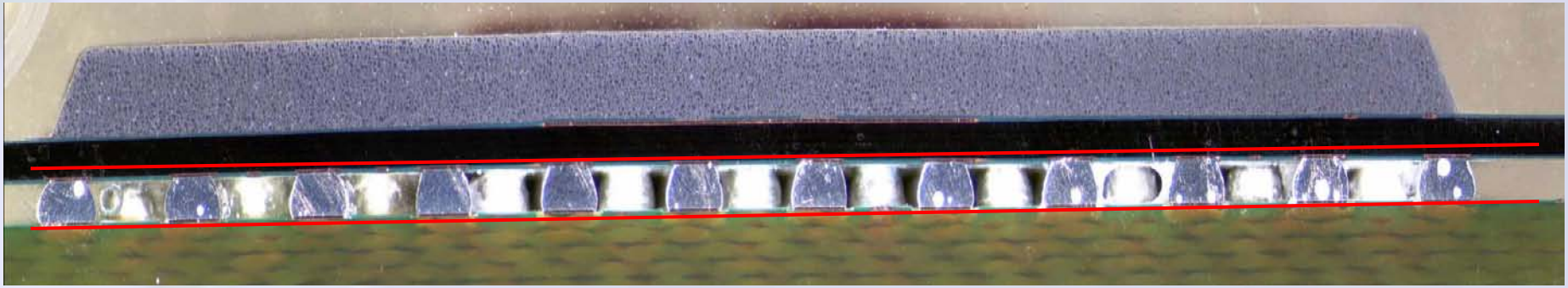
# Component Issues - Warpage

- Higher Lead Free Solder Solidification and Process Temperatures, Increases The Amount Of Thermal Expansion Mismatch Of Components Which Can Increase Amount Of Component Warping During Assembly Process

- May Require Redesign Of Package (Material Selection) For Thermal Mass And Expansion Balance.



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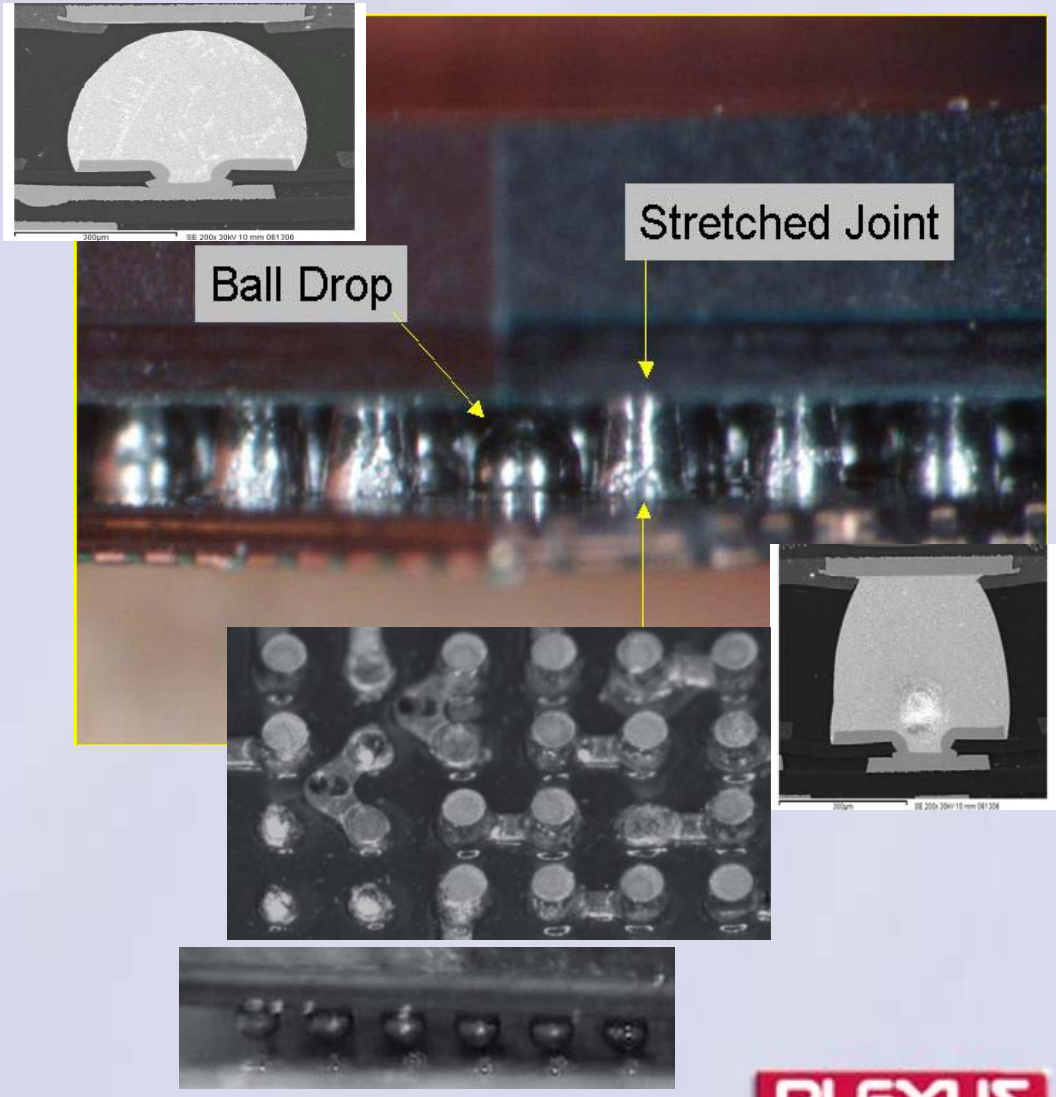
# Component/PCB Warpage Impacts

## Split Planes/Unused Pad Removal:

- Localize Changes In Thickness/Coplanarity Of PCB
- Potential Opens From Tilted Components (Teeter-Totter Effect)
- Potential Opens From “Dropped” Solder Connection
- Potential Reduced Reliability From Stretched Solder Joints




Some Photos Courtesy of Amkor

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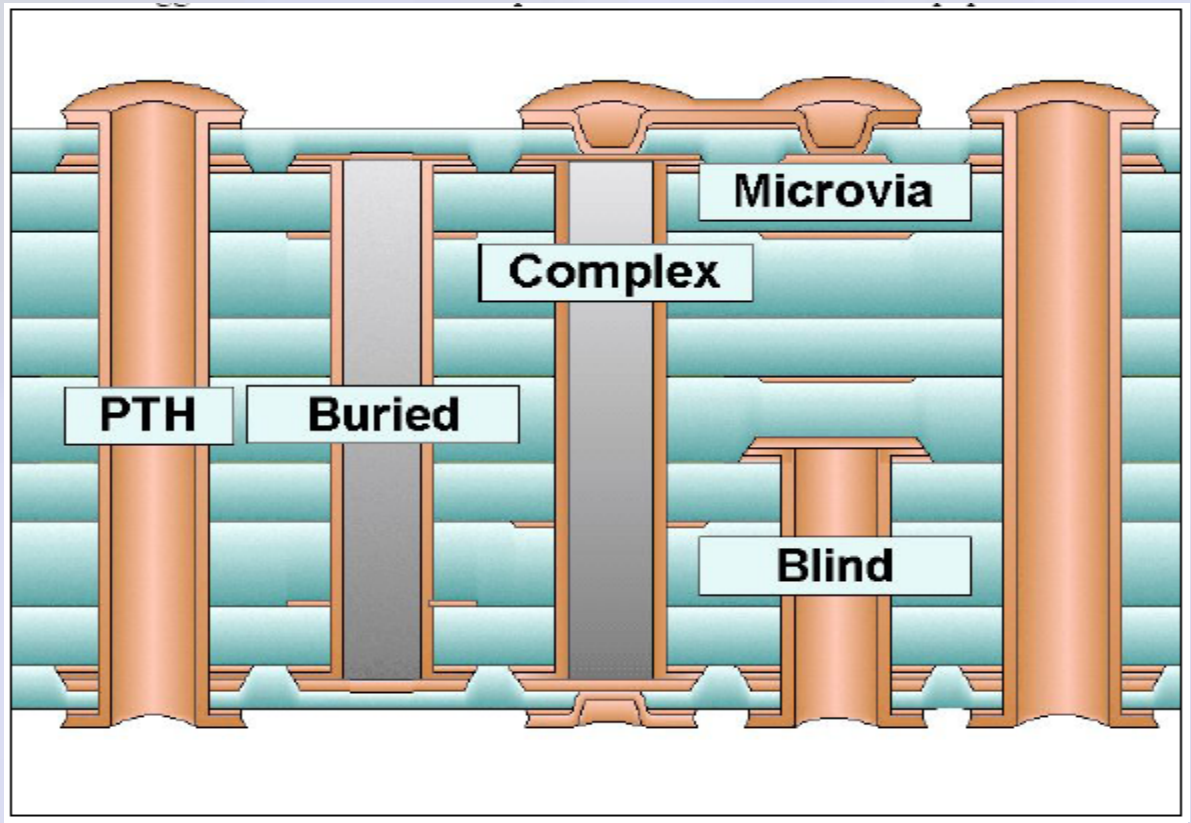
# Impacts of Via Design on Assembly

- Placement And
  - Types Of Vias In Pad Can Affect Assembly Solder Joint Formation
    - More Of An Impact On Smaller Components And/Or Lower I/O Count




Design and Construction Affects on PWB Reliability, Paul Reid, IPC Apex Proceedings 2012.

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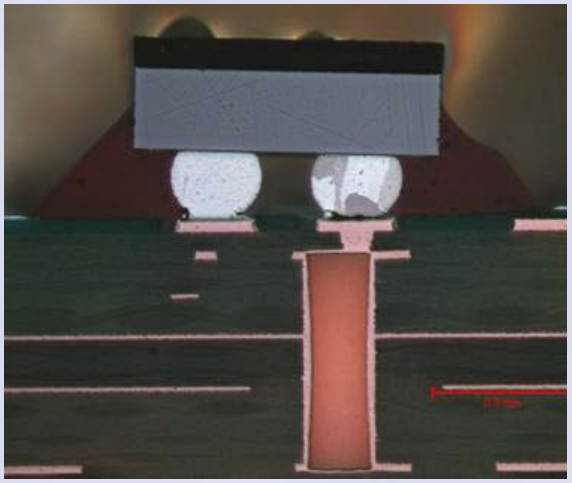
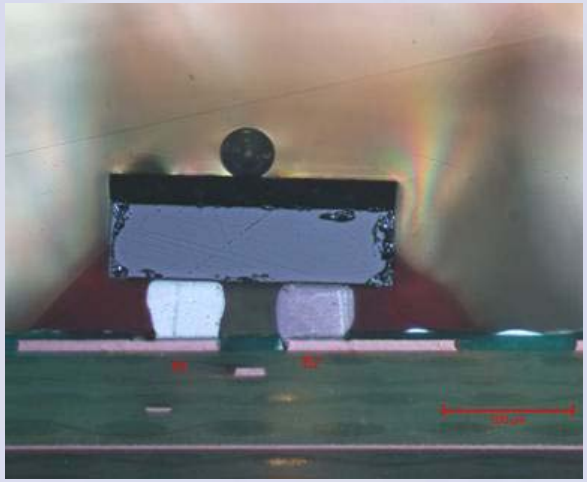
# Stacked Via Holes

- Placement Of Stacked Vias Under Devices May Create Slight Mounting Pad Height Differences
  - More Of An Impact On Smaller And/Or Lower I/O Count





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# PCB Finish Coatings

- **Hot Air Solder Level (HAL or HASL)**
  - ❖ Immerse PCB in Molten Solder, Hot Air Stripped Excess Solder.
  - ❖ Tin-Lead Coating (Sn63/Pb37, Sn60/Pb40)
  - ❖ Lead Free Coating (SnCu, SnCuNi)
  - ❖ Vertical, Horizontal Process
- **Immersion Gold (Gold Flash)**
  - ❖ 0.05 µm - 0.13 µm ( 2 - 5 µ") Electroless Gold over
  - ❖ 2.5 µm - 5.0 µm ( 100 - 200 µ") Nickel
- **Organic Surface Preservative (OSP)**
- **Immersion Tin**
- **Immersion Silver**
- **Immersion Palladium**

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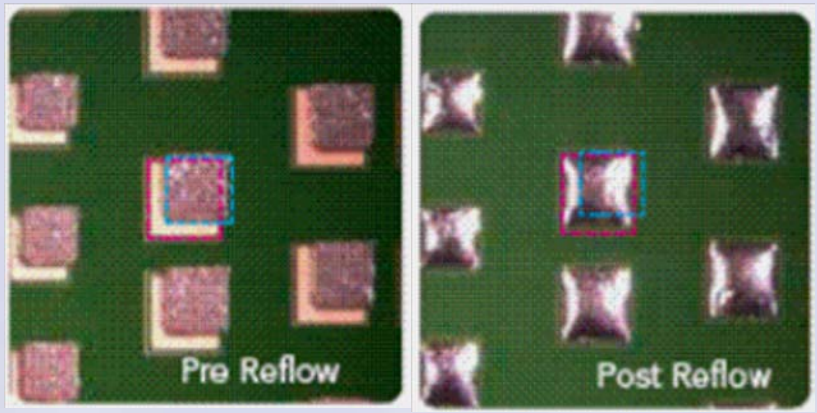
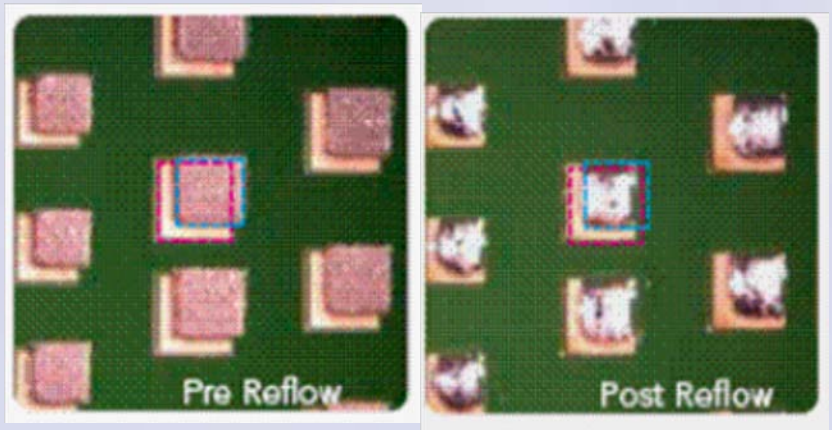
# Lead Free Solder Spread

- Stencil Alignment of Solder Paste To Pad Tolerance May Be Critical To Good Manufacturing Yields
  (Dependant Upon PCB Surface Finish)
- Example – OSP Finish




Tin-Lead Paste




Lead Free Paste

Alpha Metals, SMT Mag Webcast, Jan 2006

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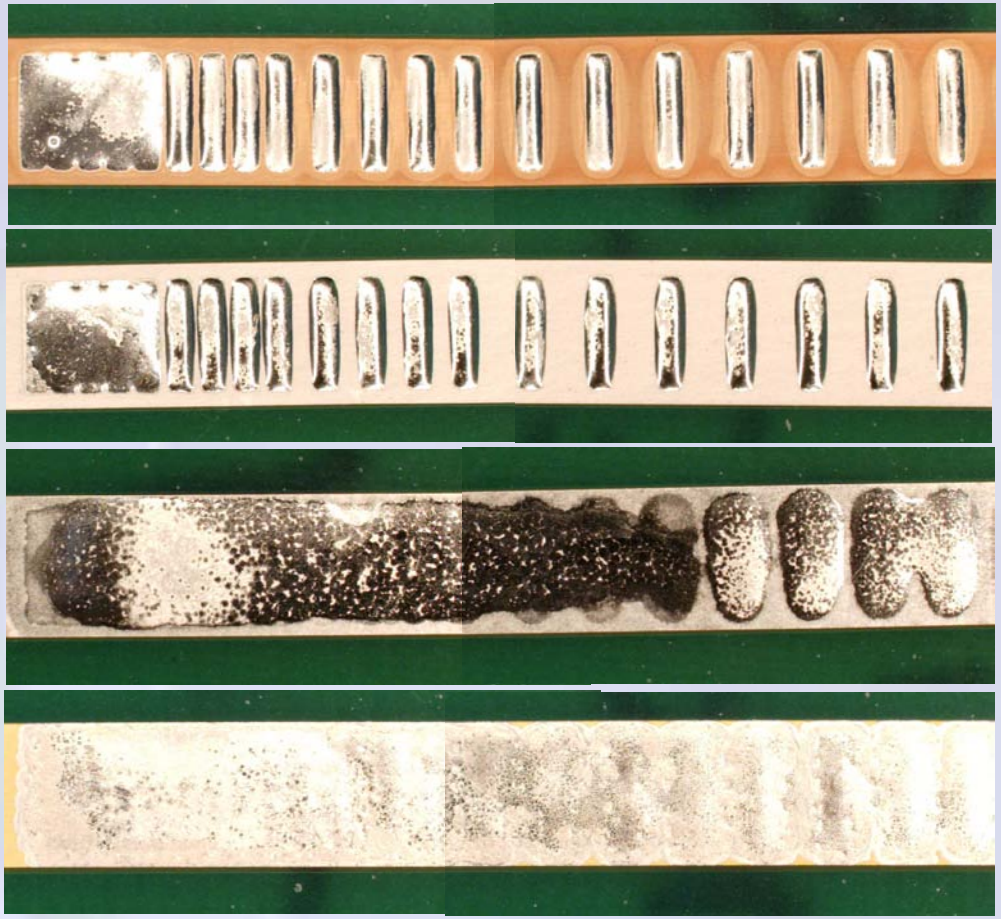
# PCB Finish Vs Solder Spread



– OSP

– Immersion Silver

– Immersion Tin

– ENIG

**Amount Of Lead Free Solder Wicking Is Dependant Upon Finish**

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# Process Control Issues

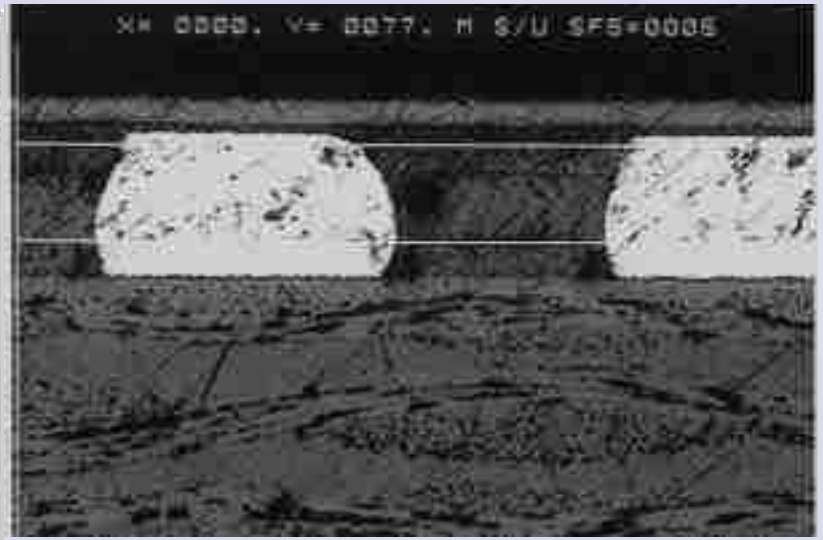
Component Attachment, Height Critical

- Solder Volume
- Land Pattern Design
- Component Interconnect Type
- Component Mass
- Component Soldered in Compression
- Component Soldered in Tension

# BGA vs CSP Z-Height

## Comparison

**256 I/O  1.27mm pitch vs.  46 I/O  .75mm pitch**



Potential Issues:

Paste Volume

Part Flatness

Board Warpage

Same Scale

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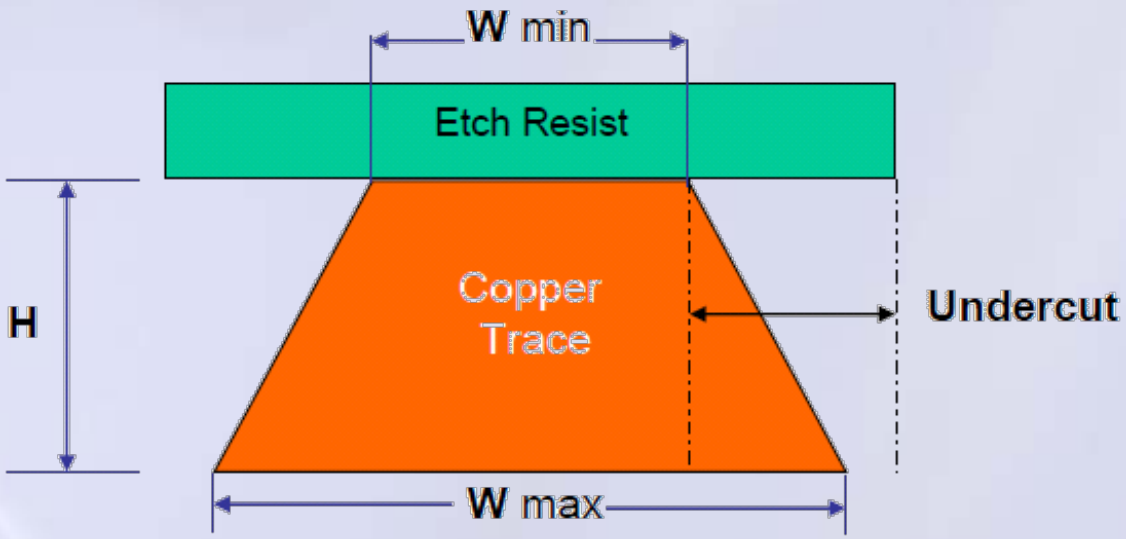
# Copper Etch Process

- **H = Height of Copper Trace**
- Etch Factor = 2H / (**W max - W min**)
- Etch Factor Should Be Larger Than 1.0

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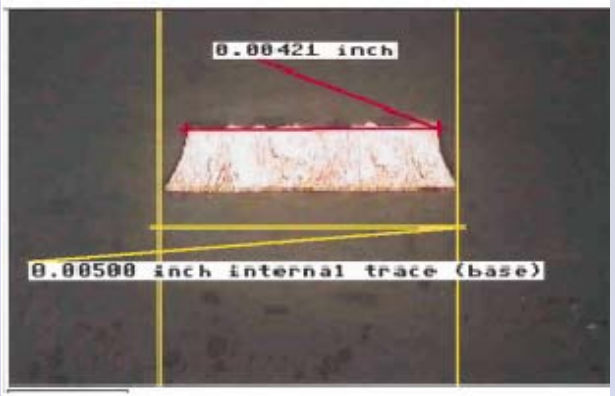
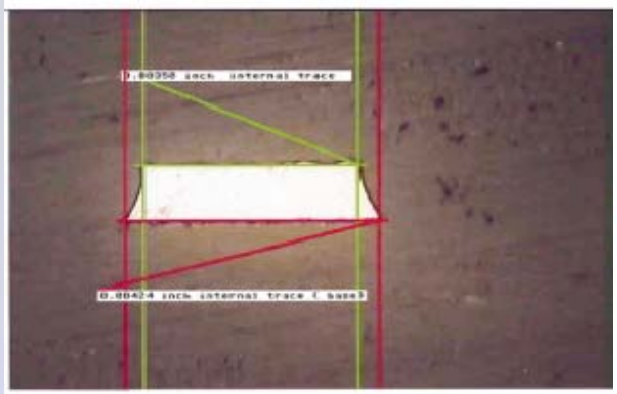
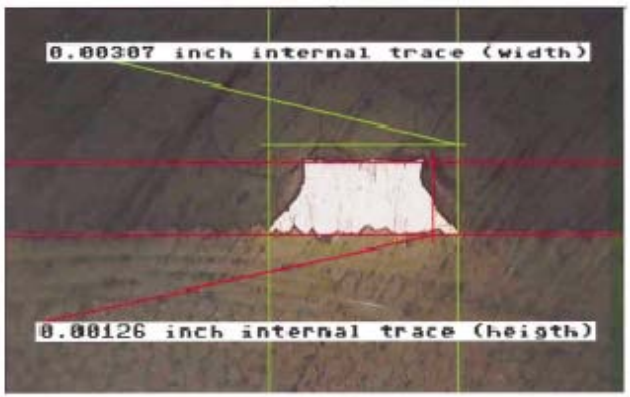
# Etched Trace Design Considerations




0.005” Trace 1 oz copper



0.004” Trace 1 oz copper




0.003” Trace 1 oz copper

- Thinner Copper Produces More Precise Geometries on Lines Less Than 0.005” in Width
- Actual Conductor Shape is Close to a Trapazoid
- Copper Thickness is Slightly Reduced After PCB Processing

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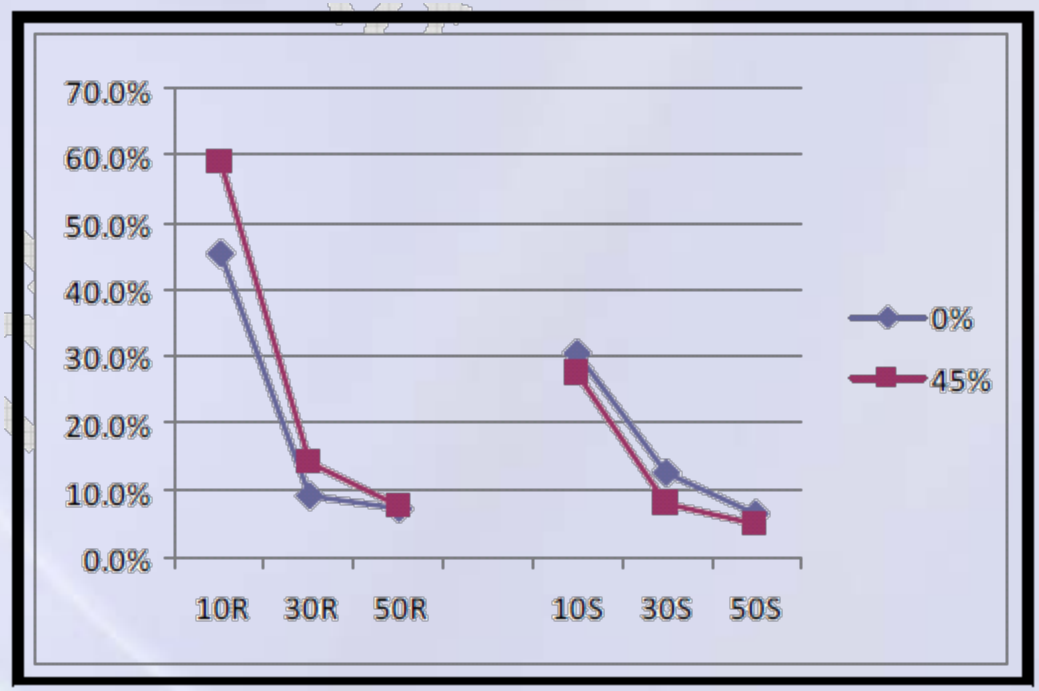
# Pad Size Reduction

Current Procedures For Applying Uniform Etch Compensation Values Across All Surface Features Are Inadequate.

Below Illustrate A Near Exponential Reduction In Pad Size As The Pad Gets Smaller, For Both Round And Square Pads In Either Orientation.




*Percentage Reduction by Pad Size*

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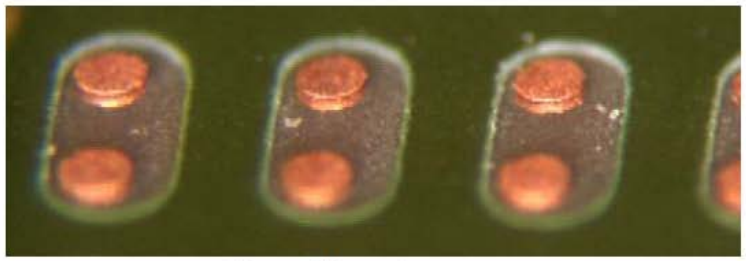
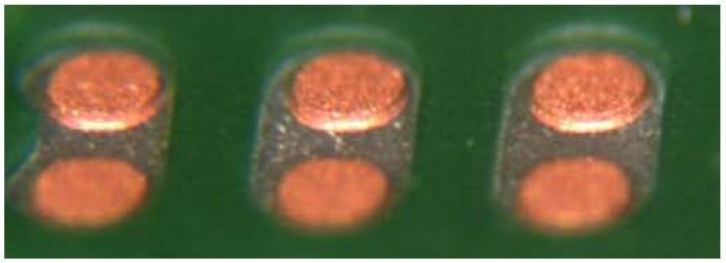
# PCB Fabricator Variation

## Pad Size Comparison

– Same design data may not yield same PCB pads sizes.



Supplier A



Supplier B

DFM Rules for Smartphones: An Analysis of Yield on Extremely Dense Assemblies, Jimmy Chow et al., IPC Apex Proceedings 2012.

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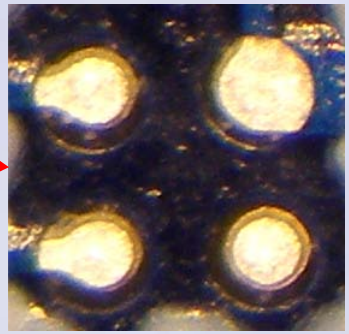
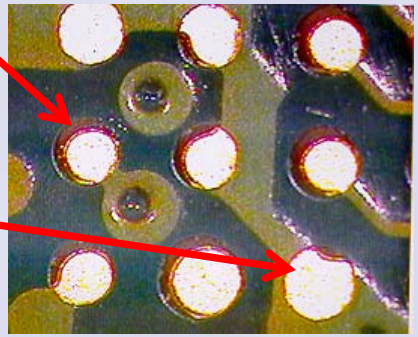
# Solder Mask Opening Design

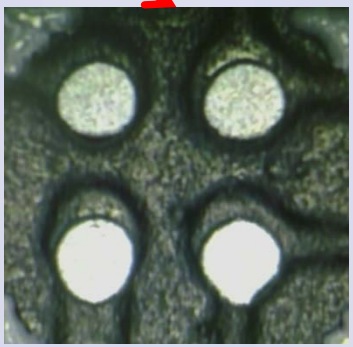
## Pad Geometries

- Non-Solder Mask Defined (NSMD)
  - Size of Pad Defined By Copper Pad and Interconnections (Variable Size)
  - Solder Encapsulates Pad
  - Limited to Components With Lead Pitch Greater Than 0.4mm



- Solder Mask Defined (SMD)
  - Size of Pad Defined By Solder Mask Opening (Uniform Size)
  - Solder Covers Exposed Pad (Fills Opening)
  - Required For Components With Lead Pitch 0.4mm or Less.
  - Preferred for Leadless Array Devices Like LGA's, Multi-row QFN's, etc.





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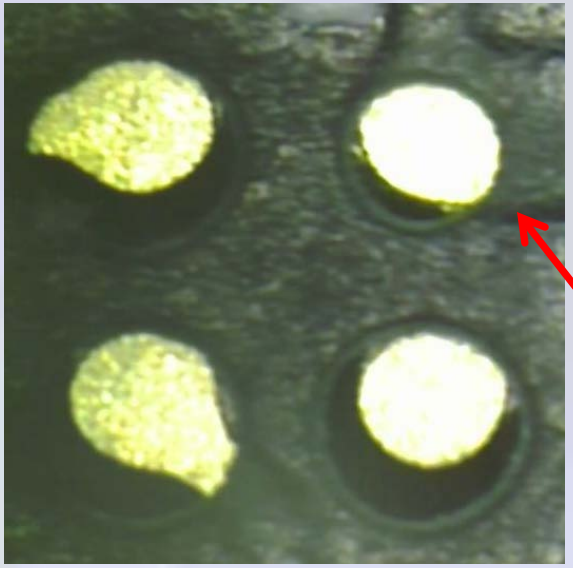
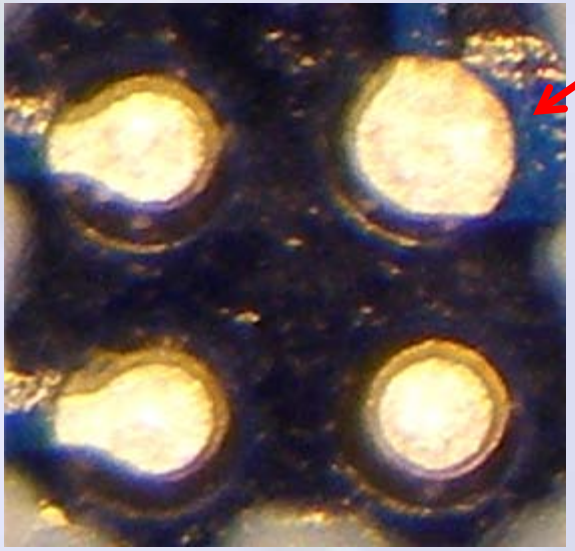
# PCB Fabricator Variation





- Solder Mask Fabrication Consistency
  - Fabrication Note Interpretation
    - “No Solder Mask Permissible On Pads Unless Provided This Way On Supplied Artwork ”
    - (Selective Solder Mask Opening Changes Between PCB Suppliers)

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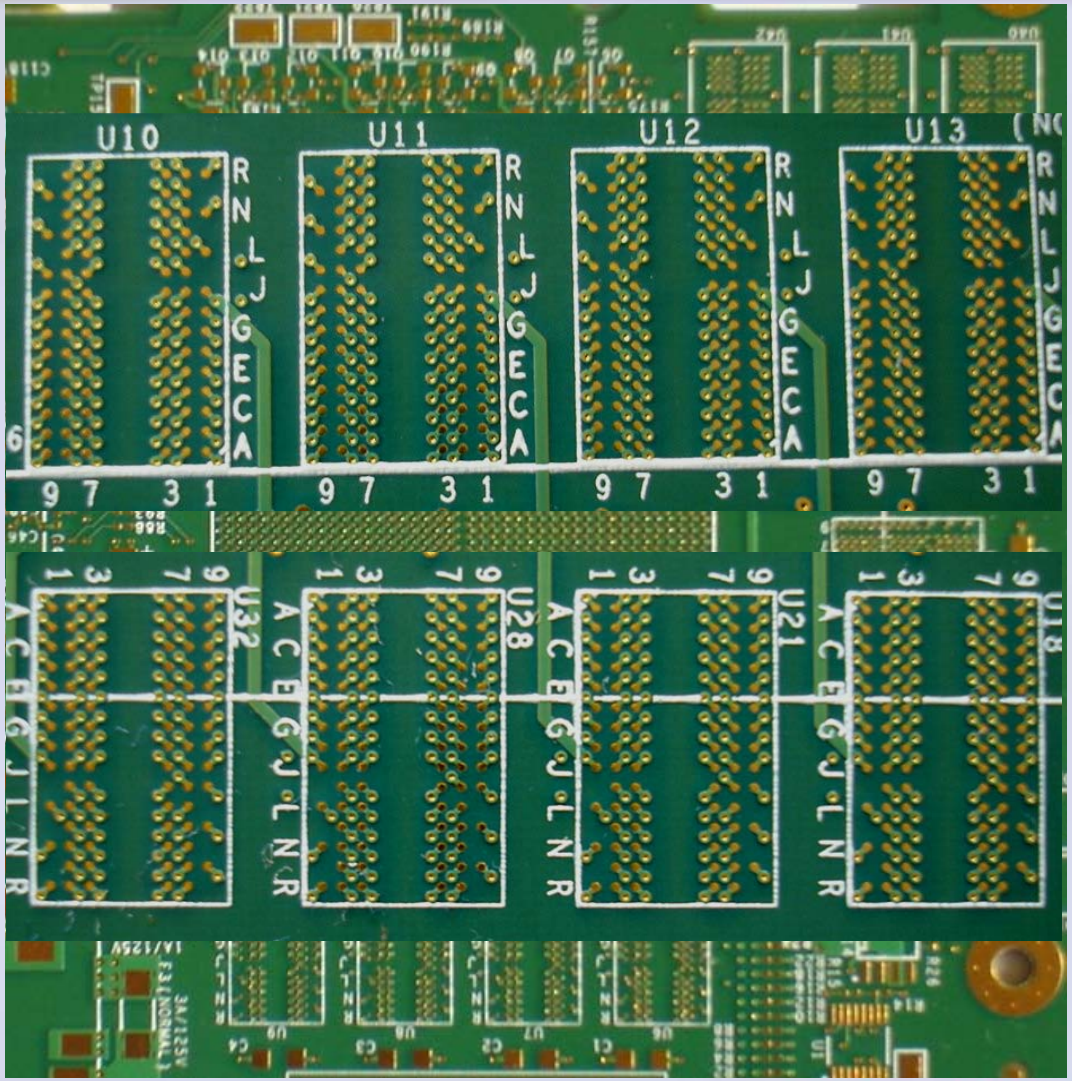
# Silk Screen Design

## Low Component Stand-off Height

- Tilted Component
- Open Joints (standoff from PCB)
- Misalignment

## Component Types

- Leadless
  - QFN, DFN, Passives, etc.
- Fine Pitch Area Array
  - BGA, WL-CSP, CSP, etc.

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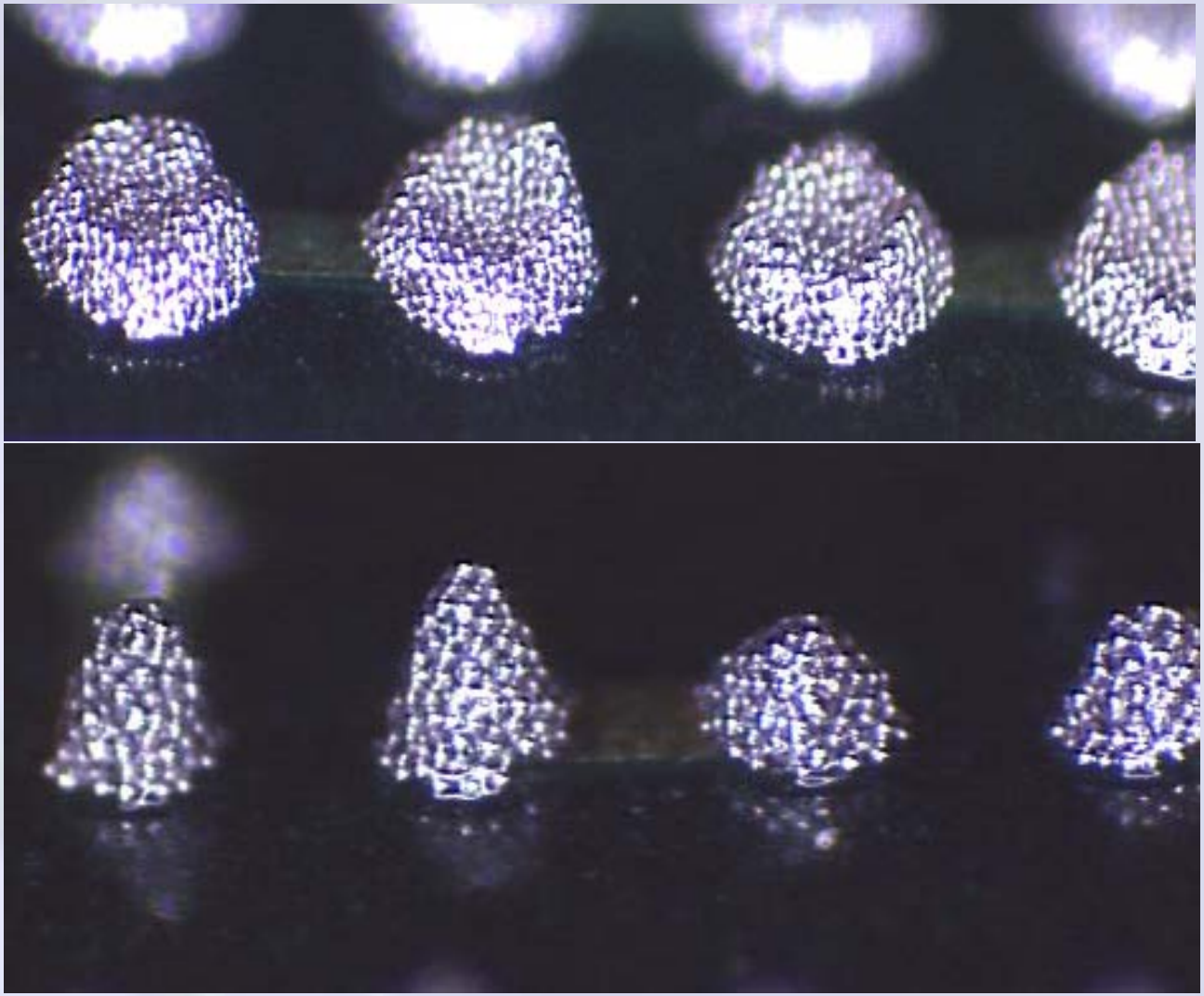
# Solder Paste Printing



- Low Aspect Area Ratio Printing
- High Aspect Area Ratio Printing

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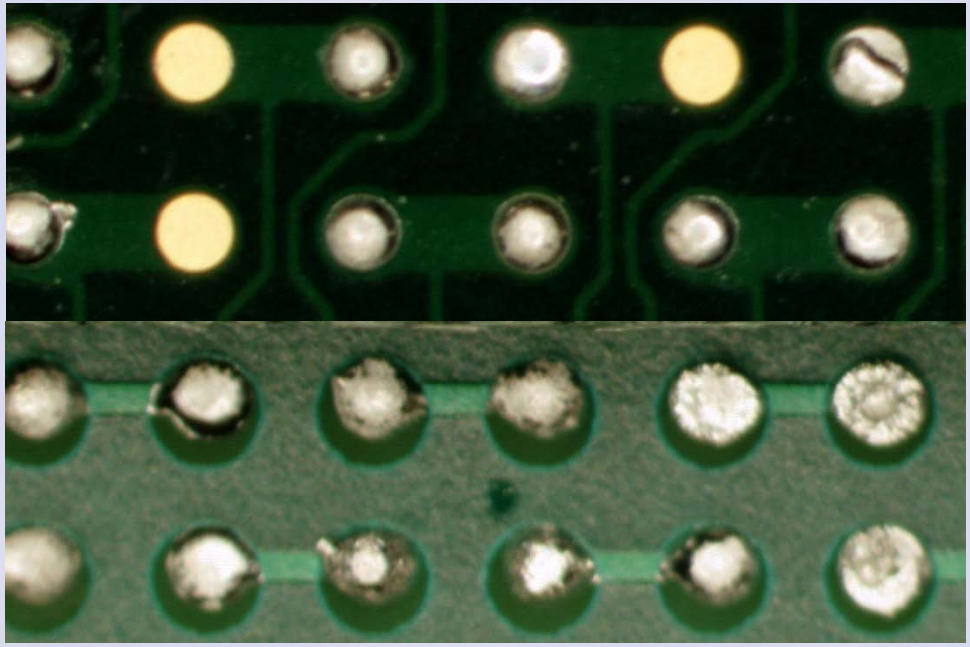
# Solder Paste Printing Volume

Leadless Device Usage Increase (DFN, QFN, LCC LGA) & Ultra-fine Pitch Components Impacts:

- Tighter Tolerance On Solder Paste Volume – Thinner Stencil
- Increased Uniformity Of Paste Volume Across Component (Pad to Pad)
- Paste Volume/Pad Trace Egress Direction Impact
  - Some Package Types Are More Sensitive Than Others



**Open/Unwetted LGA Solder Connection**

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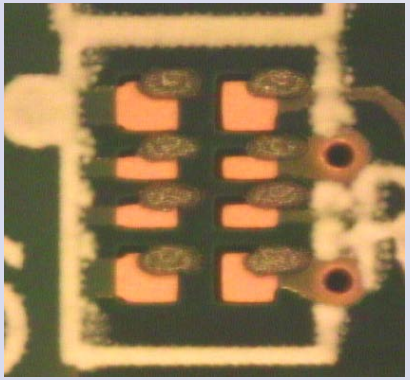
# Assembly Issues

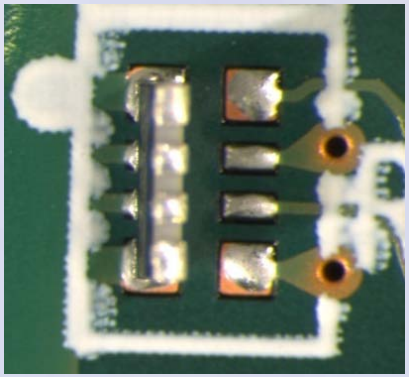
- Stencil Design
  - Registration To PCB
    - Decrease PCB/Panel Size
    - Modify Pad/Aperture Size
  - Component Mounting Restrictions
    - Minimum Solder Paste - Minimal Solder Pedestal
    - Paste Location on Pad - Improve Component Alignment

# Stencil Tolerances

## Artwork Feature Positional Tolerances Increase

- Fabrication Tolerances Artwork Registration
  - Etched Feature Position
  - Etched Feature Size
  - Etched Feature Quality
  - Etched Feature Directional Etch
- Stencil Print Directional Compensation Orientation





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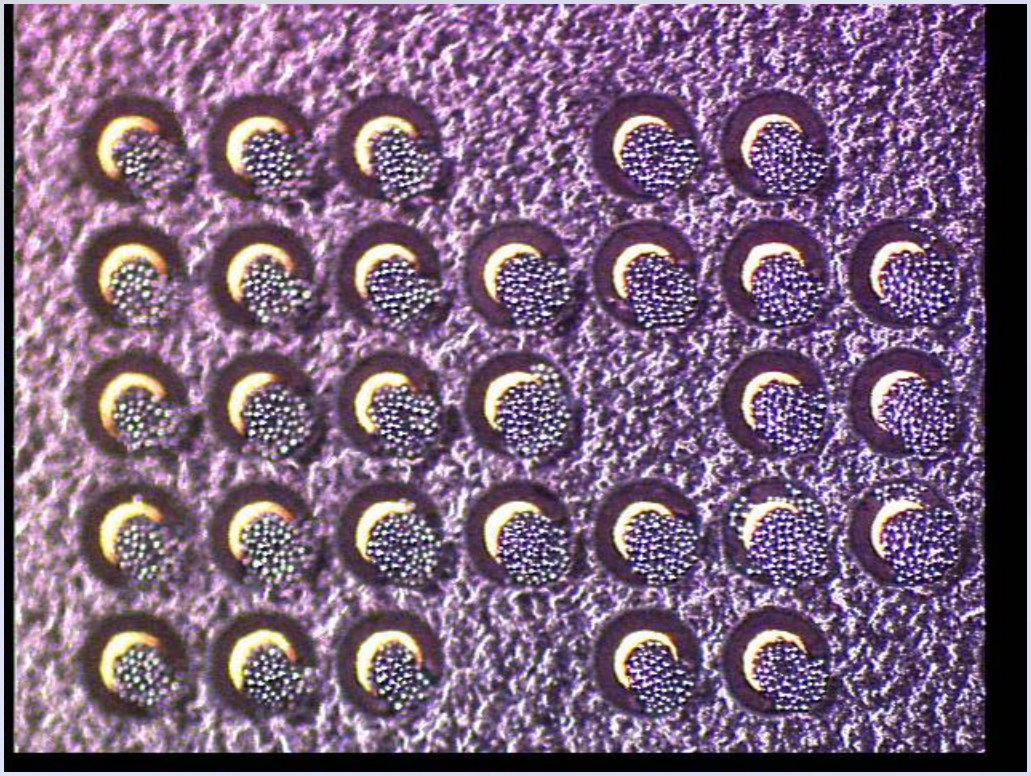
# Printed Paste Offset



•Printing Process Positional Tolerances
Windows Decrease With Decrease in CSP Pitch

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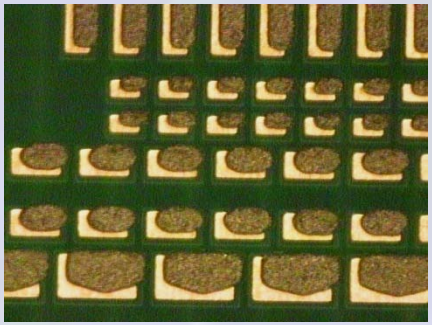
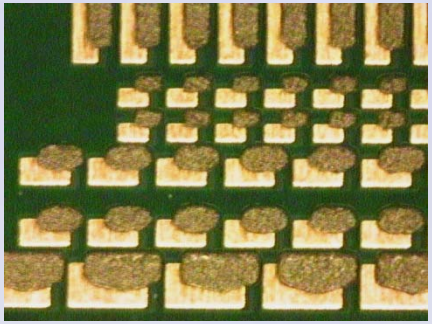
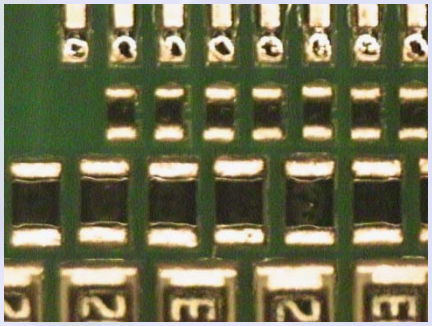
# Stencil To PCB Alignment

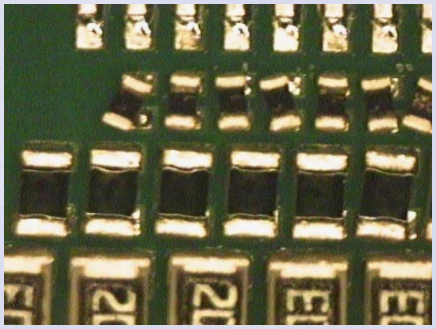


- Smaller Components Decrease Total PCB & Assembly Process Tolerance
- Minor Misalignment Can Impact Process Yields





3 mil



6 mil

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# Offset Paste – Normal Placement

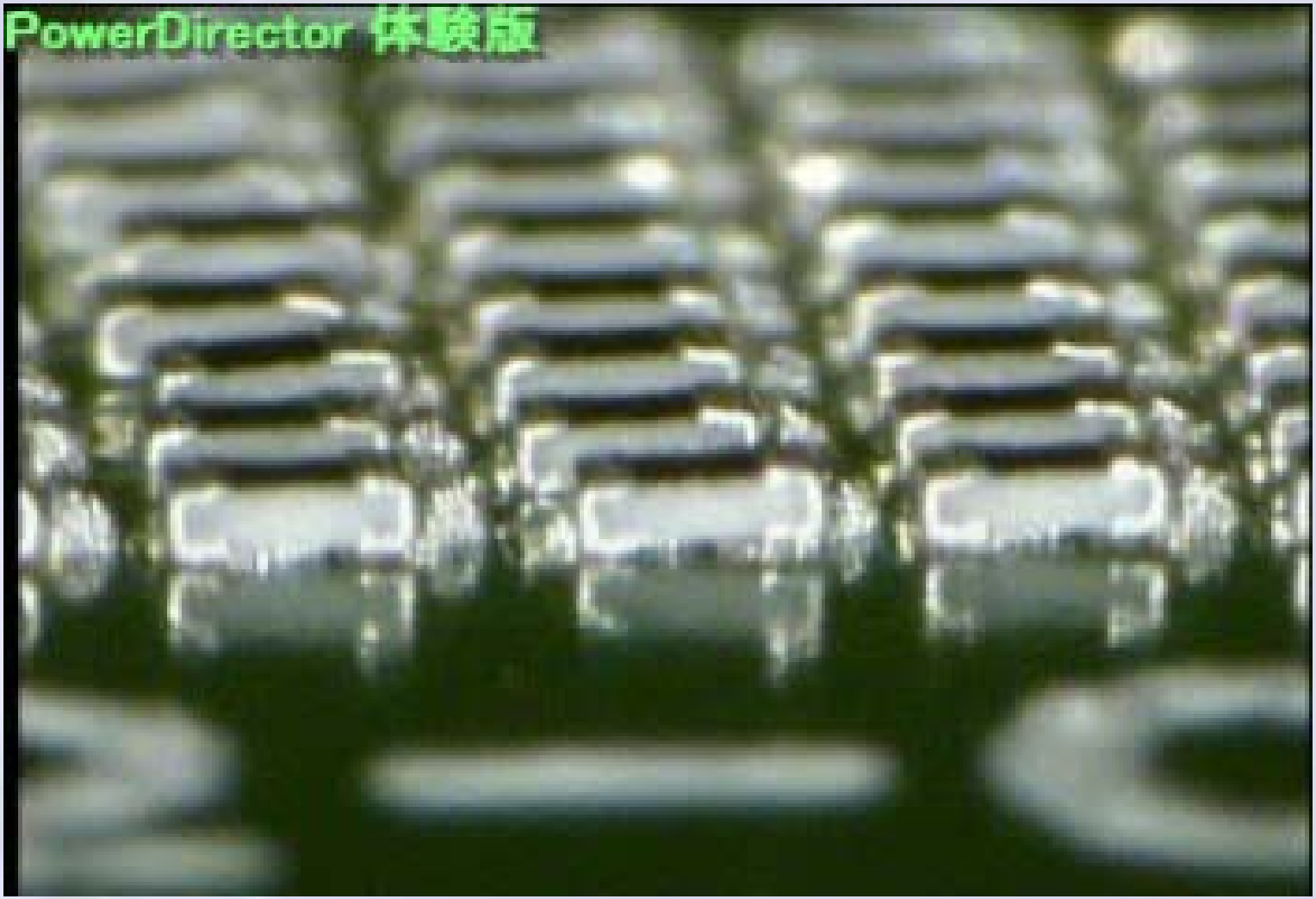


Photo Courtesy of Juki Automation

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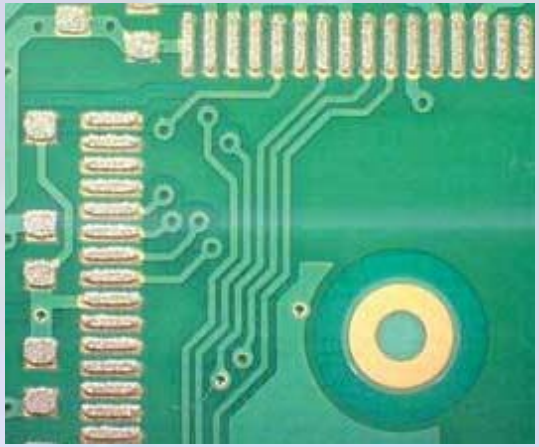
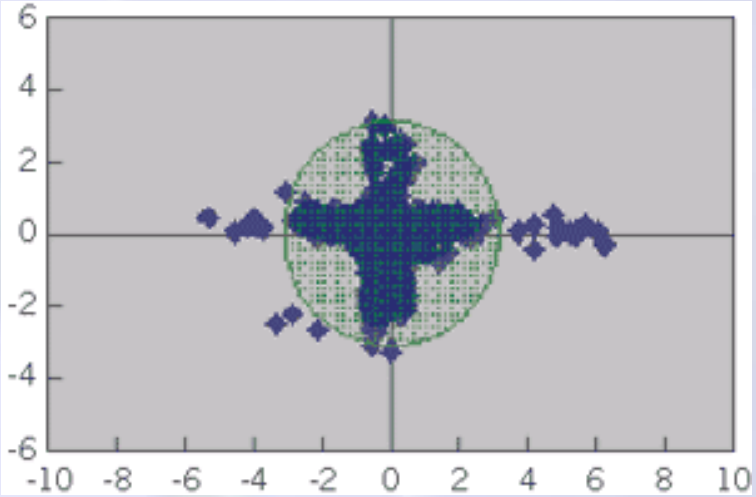
# Match Tooling Design To Parts

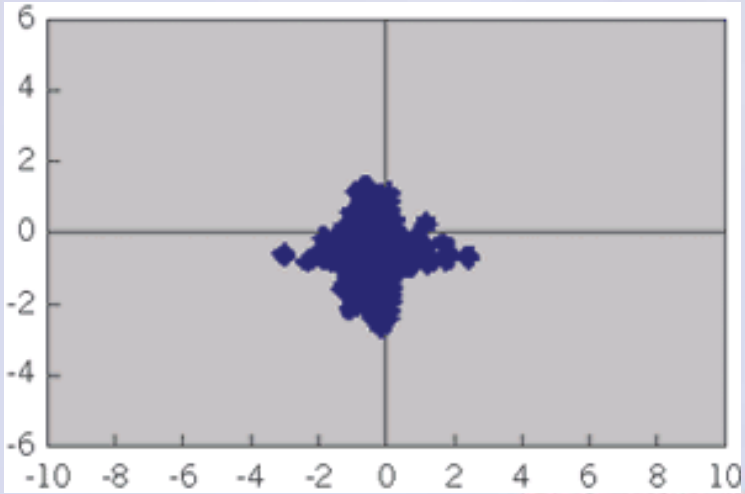


- Normal Manufacturing Process Variability May Exceed Allowable Assembly Process Tolerance For High Yield, Reliable Assembly
- Matched Tooling (Stencils) To Materials (PCB) May Be Required

PCB to Stencil Pad Positional Deviation Measurements No Adjustments




PCB to Stencil Pad Positional Deviation Measurements With Scaling Adjustments

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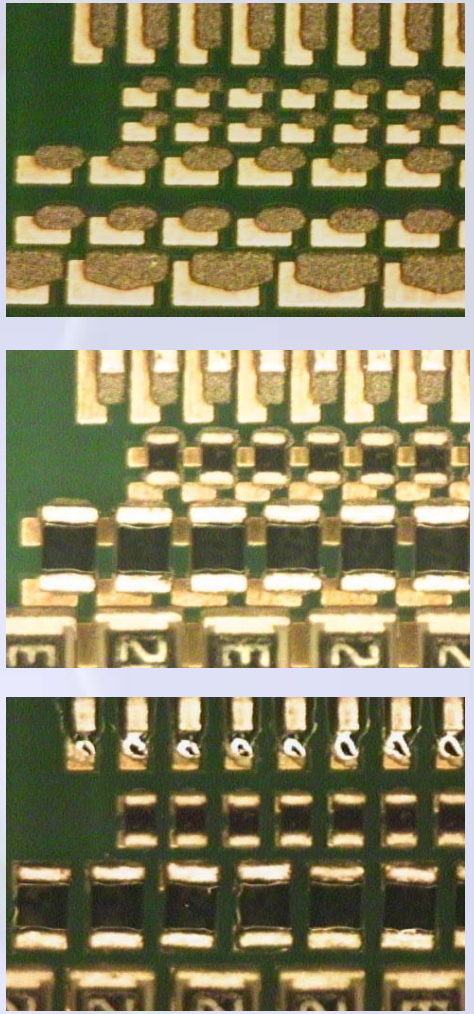
# Match Placement To Paste



- Slight Offset Of Solder Paste And Component Placement May Improve Soldering Yields
  - Paste and Placement Must Have Same Offset
  - Tombstone Passives
  - BGA Voiding

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# Matched Offset – Paste & Part

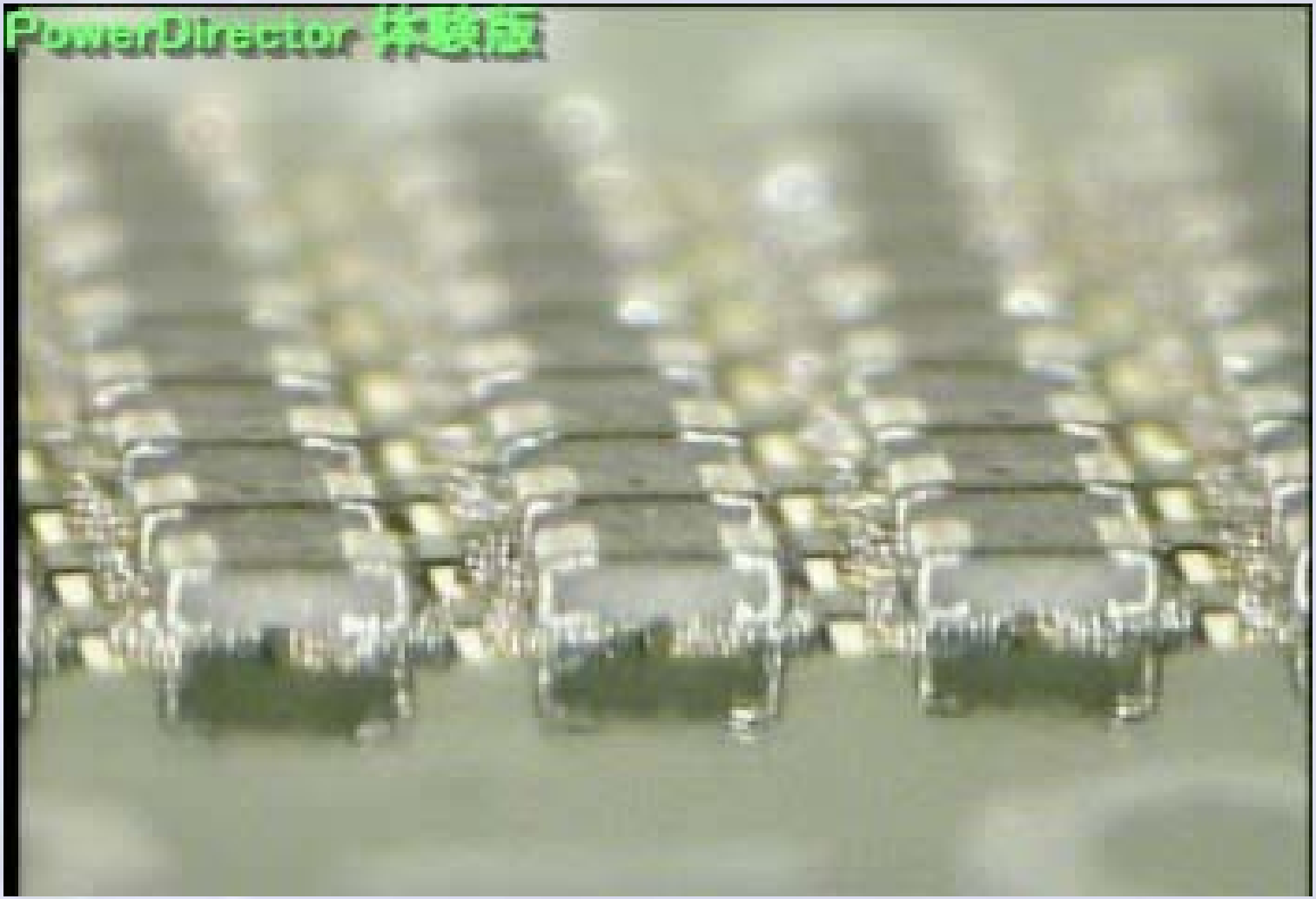

Photo Courtesy of Juki Automation

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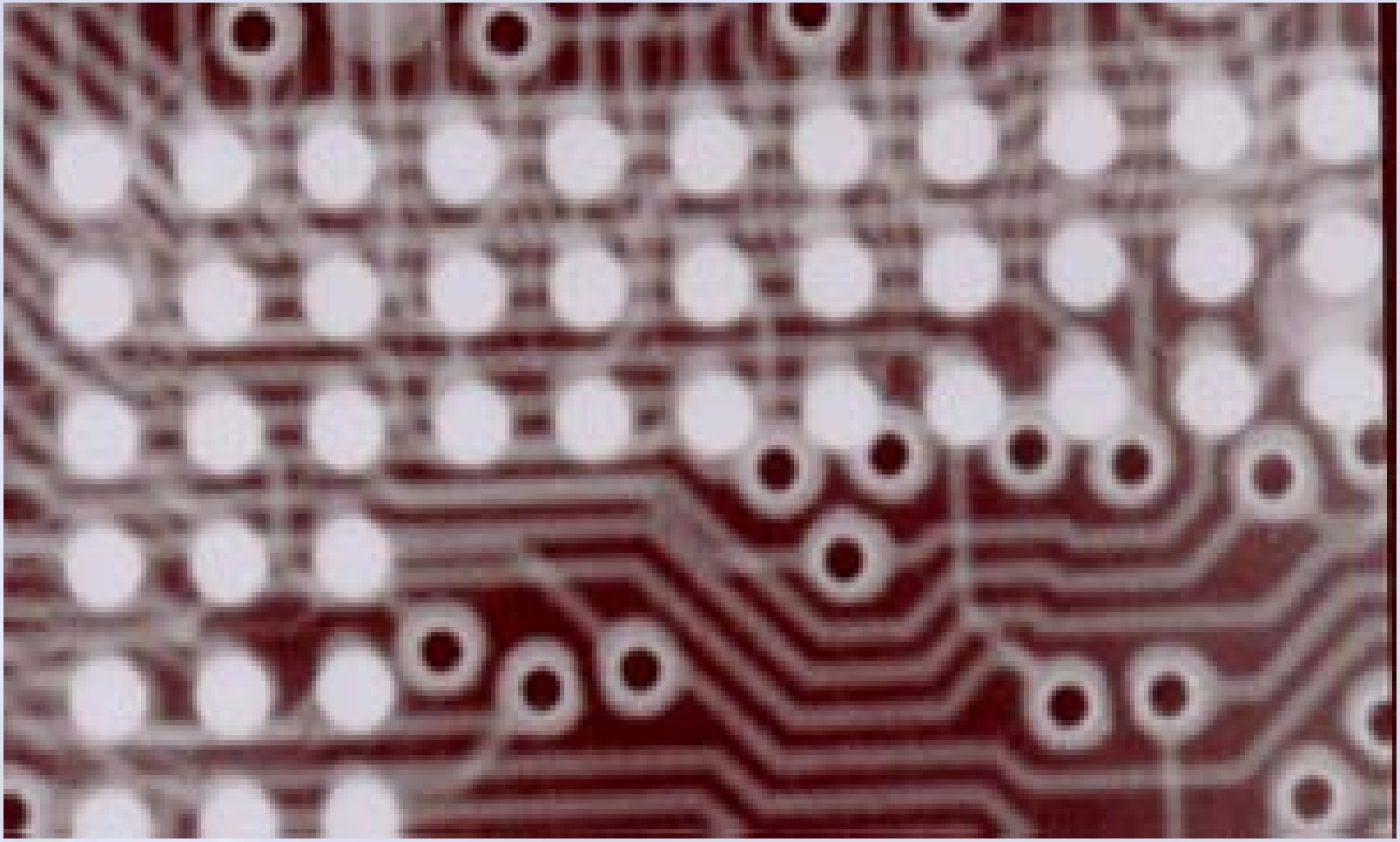
# Part Offset



X-ray of Component Offset in Solder Paste

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# Warpage & Thermal Profile Issues

## May Require Change In Production Process

Reflow Profile To Bridge PCB Warpage Gap.

(Decreased Thermal Change Rate And Delta T Vertically In PCB – Reduce Surface To Cooler Location Temperature Delta - TCE Induced Warpage)

Large ΔT across Board

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# Closing Thought

"We can't solve problems by using the same kind of thinking we used when we created them."

Albert Einstein

**Don't Forget About Reflow Process Induced Warpage/Coplanarity Issues.**

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